

# A 1.9 GHz Low Noise Amplifier

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*Abstract*—This paper describes a 1.9 GHz, 25 mW, 0.25  $\mu\text{m}$  CMOS Low Noise Amplifier (LNA), intended for use in a DECT (Digital Enhanced Cordless Communications) Receiver. The LNA has been simulated with Cadence Spectre and the results show that it provides a gain of more than 15 dB, for a noise figure of 2dB, and an input referred IP3 of  $-5\text{dBm}$ . We present the LNA architecture and the circuit analysis along with some considerations on the layout of the inductors used, and the results of the simulations.

## I. INTRODUCTION

THE goal of this project was to design a low noise amplifier (LNA) for a receiver that meets the Digital Enhanced Cordless Telecommunications (DECT) standard [1]. "DECT is a flexible digital radio access standard for cordless communications in residential, corporate, and public environments." The LNA amplifies a weak signal coming from an antenna and which is processed through an off-chip filter. The amplified output from the LNA is then fed into a mixer. The LNA must be able to meet the specifications listed in table I. It was implemented in a 2.5 V, 0.25  $\mu\text{m}$ , 5 metal layers process. A fully differential design was used to insure adequate rejection of the noise and the interfering signals travelling through the common substrate. Also, we considered a CMOS implementation because the push toward high level of integration and low cost have made CMOS solutions in RF analog design an attractive alternative to such processes as GaAs and BiCMOS. The technology scaling in CMOS has increased the transistor's cutoff frequency,  $\omega_T$ , which allows improved noise performance of the CMOS circuit. Research in recent years on CMOS LNA design has investigated various features such as topology, improvement of low noise figure, high power gain, low power consumption, and high linearity. All these features were considered in our LNA design with the exact specifications shown in table I. The choice of our particular design is based on the discussion by Schaeffer and Lee ([2], [3]).

## II. CIRCUIT DESCRIPTION AND ANALYSIS

### A. LNA Architecture

In the design of low noise amplifiers, there are several common goals. These include minimizing the noise figure of the amplifier, providing gain with sufficient linearity and providing a stable 50 $\Omega$  input impedance to terminate an unknown length of transmission line which delivers signal from the antenna to the amplifier. A good input match is even more critical in the DECT system since the pre-select filter which precedes the LNA is often sensitive to

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TABLE I  
CHARACTERISTICS AND SPECIFICATIONS OF THE LNA.

Features	Specifications
Low noise	$NF < 2.5 \text{ dB}$
High linearity	$IIP3 > -10 \text{ dBm}$
Moderate gain	$A_v > 15 \text{ dB}$
Low power consumption	$P < 25 \text{ mW}$
Narrow band design	$f = 1.9 \text{ GHz}$
Other characteristics	2.5V Power supply 0.25 $\mu\text{m}$ process Fully differential 50 $\Omega$ input impedance

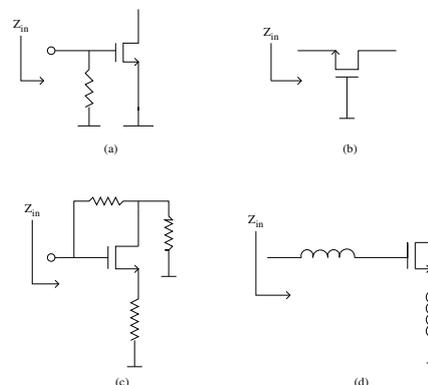


Fig. 1. Common LNA architectures. (a) Resistive termination, (b)  $1/g_m$  termination, (c) shunt-series feedback, (d) inductive degeneration

the quality of the terminating impedance. The additional constraint of low power is imposed in portable systems.

With these goals in mind, we will first focus on the requirement of providing a stable input impedance. To present a known resistive impedance to the external world, a number of circuit topologies as shown in figure 1 were examined and we then narrowed the field of contenders by evaluating their noise performance.

The input impedance of a MOSFET is inherently capacitive, so providing a good match to a 50 $\Omega$  resistance without degrading noise performance would appear to be difficult. Simply putting a 50 $\Omega$  resistor across the input terminals of a common source amplifier as shown in figure 1(a) adds thermal noise while attenuating the signal ahead of the transistor. This produces unacceptably high noise figures. Another method as shown in figure 1(b) for realizing a resistive input impedance is to use a common-gate configuration since the resistance looking into the source terminal is  $\frac{1}{g_m}$ ; a proper selection of device size and bias current can provide the desired 50 $\Omega$  resistance. But the noise figure of this

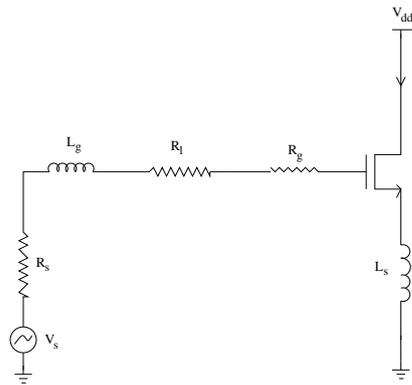


Fig. 2. Equivalent circuit for the input stage.

configuration would be high for high frequencies due to the gate current noise of the transistor. The third configuration (figure 1(c)) uses a resistive shunt and series feedback to set the input and output impedances of the LNA. But this has high power dissipation compared to others with similar noise performance due to the fact that shunt-series amplifiers of this type are naturally broadband, and hence techniques which reduce power consumption through LC tuning are not applicable. It also requires on-chip resistors of reasonable quality, which are generally not available in CMOS technologies. We found that the fourth architecture shown in figure 1(d), employing an inductive source degeneration, is the best method. With such an inductance, a real term in the input impedance can be generated without the need of real resistances which degrade the noise performance. Tuning of the amplifier input then becomes necessary, making this a narrow band approach which is favorable for our application.

To simplify the analyses, if we consider a device model that includes only a transconductance and a gate-source capacitance, it can be seen that the input impedance of the circuit is

$$Z_{in} = sL_g + \frac{1}{sC_{gs}} + g_{m1} \frac{L_s}{C_{gs}} = sL_g + \frac{1}{sC_{gs}} + \omega_T L_s \quad (1)$$

where  $\omega_T = \frac{g_{m1}}{C_{gs}}$

Hence, the input impedance is that of a series RLC network, with a resistive term that is directly proportional to the inductance value. At the series resonance of the input circuit, the impedance is purely real and proportional to  $L_s$ . By choosing  $L_s$  appropriately, this real term can be made equal to  $50\Omega$ . The gate inductance  $L_g$  is then set by the resonance frequency once the  $L_s$  is chosen to satisfy the criterion of a  $50\Omega$  input impedance.

The equivalent circuit for the input stage of the amplifier is shown in figure 2. The noise figure of the LNA can be computed by analyzing this circuit.  $R_l$  represents the series resistance of the inductor  $L_g$ , and  $R_g$  is the gate resistance of the NMOS device. Analysis based on this circuit neglects the contribution of subsequent stages to the amplifier noise figure. This is justifiable provided that the first

stage possesses sufficient gain, which is true. The overlap capacitance  $C_{gd}$  is neglected for simplicity. As we have used a cascoded first stage, we are ensured that this approximation will not introduce serious errors.

The noise factor for an amplifier is defined as

$$F = \frac{\text{Total output noise}}{\text{Output noise due to the source}}$$

To evaluate the output noise, we first evaluate the transconductance of the input stage. With the output current proportional to the voltage on  $C_{gs}$ , we have

$$G_m = g_{m1} Q_{in} = \frac{\omega_T}{\omega_0 R_s (1 + \omega_T \frac{L_s}{R_s})} = \frac{\omega_T}{2\omega_0 C_{gs}} \quad (2)$$

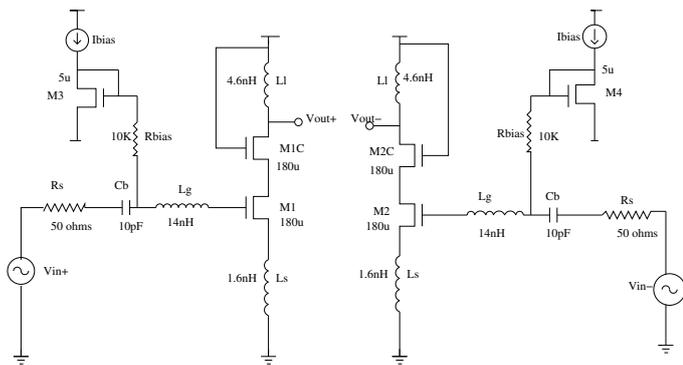
which is valid at the series resonance  $\omega_0$ , where  $Q_{in}$  is the effective Q of the amplifier input circuit.  $R_l$  and  $R_g$  have been neglected relative to the source resistance. As seen, the transconductance of this circuit at resonance is independent of  $g_{m1}$  (the device transconductance) as long as the resonant frequency is maintained constant. If the width of the device is adjusted, the transconductance of the stage will remain the same as long as  $L_g$  is adjusted to maintain the fixed resonant frequency. If we narrow  $M_1$  without changing any bias voltages, the device transconductance would also shrink by the same factor, and the inductances would have to increase (by the same factor) to maintain resonance. Since the ratio of inductance to capacitance increases, the Q of the input network must increase. The increase in Q cancels precisely the reduction in device transconductance, so that the overall transconductance remains unchanged.

Using equation 2 for the transconductance, the output noise power density due to the  $50\Omega$  source resistance and due to  $R_l$ ,  $R_g$  and the channel current noise of the first MOS device is computed. We then arrive at the following equation for the noise figure

$$F = 1 + \frac{R_l}{R_g} + \frac{R_g}{R_s} + \gamma g_m R_s \left( \frac{\omega_0}{\omega_T} \right)^2 \quad (3)$$

This equation shows that we can improve the noise figure and reduce the power consumption simultaneously by reducing  $g_m$  and without modifying  $\omega_T$  (although this is probably different from our first intuition). This can be achieved by scaling the width of the device while maintaining constant bias voltages. In this equation, the Flicker noise at this frequency is neglected with respect to the channel thermal noise. Note, however, that other sources of noise not implemented in Spectre might not be negligible, as explained in [2]. It is shown that we need to take into account the gate noise of the transistors for a more accurate estimate, and this still underestimates the noise of the real amplifier. We will not consider these other sources of noise in the following discussion.

As the amplifier is operated at series resonance of its input circuit, a reduction in  $g_m$  (and hence in  $C_{gs}$ ) must be compensated by an increase in  $L_g$ . So, better noise


 Fig. 3. Schematic of the LNA, without constant  $g_m$  biasing circuitry

performance and reduced power dissipation is obtained by increasing the Q of the input circuit resonance. However, we know that at resonance of the RLC series tank, the voltage drop at the capacitance  $C_{gs}$  will be Q times input voltage  $V_{in}$ . This has a direct influence on the distortion. We also know that for the MOSFET in the common source configuration, the third order intermodulation coefficient is proportional to the square of the gate source voltage, and therefore the distortion is proportional to  $Q^2$ . Thus, there is a trade-off between the noise performance and the distortion, as reducing the size of the transistors to decrease the noise figure increases the level of distortion.

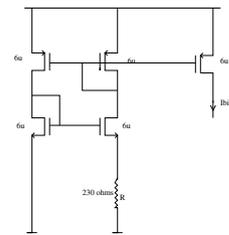
### B. Design

The basic input circuitry has already been discussed, so to complete the design largely requires only the addition of bias and output circuitry. For narrow-band applications, it is advantageous to tune out the output capacitance to increase the gain. Hence the differential LNA is as shown in Figure 3.

Cascoding transistor  $M_{1C}$  is used to reduce the interaction of the tuned output with the tuned input, and to reduce the effect of  $M_1$ 's  $C_{gd}$ . The total node capacitance at the drain of  $M_{1C}$  resonates with the inductance  $L_l$  both to increase the gain at the centre frequency and simultaneously to provide an additional level of highly desirable bandpass filtering. The input and output resonances are set equal to each other. Transistor  $M_3$  forms a current mirror with  $M_1$ , and its width is a small fraction of  $M_1$ 's to minimize the power overhead of the bias circuitry. The current through  $M_3$  is set by the constant  $g_m$  circuitry shown in figure 4 which provides constant  $g_m$  for different temperatures, in other words, a current which is directly proportional to the temperature.

The resistance  $R_{bias}$  is chosen large enough so that its equivalent noise current is small enough to be ignored. To complete the biasing, a DC blocking capacitor  $C_B$  must be present to prevent upsetting the gate-to-source bias of  $M_1$ . The value of  $C_B$  is chosen to have a negligible reactance at the signal frequency.

At the frequency of operation, 1.9 GHz, we then determined the component values and device sizes. Overall, the hand calculations gave results which were quite different


 Fig. 4. PTAT current source for constant  $g_m$  biasing.

from the simulated values. At a bias current of 4.35 mA for  $M_1$ , and for a 0.25  $\mu\text{m}$  process, we have an  $L_{eff}$  of approximately 0.18  $\mu\text{m}$  and a  $C_{ox}$  of 5.95 fF/ $\mu\text{m}^2$ . We then found out the width of transistors  $M_1$  and  $M_2$  to be approximately 180  $\mu\text{m}$  for optimum noise performance. The  $\omega_T$  is approximately  $230 \times 10^9$  rad/s for a bias current of 4.35 mA and for a transistor of this size in this technology. Having a value for  $\omega_T$ , we next find the value of the source degeneration inductance. To generate a real part of 50 ohms,  $L_s$  was found to be 1.64 nH, a value that is realized as either bondwire or as an on-chip planar stacked spiral inductor. In order to then compute  $L_g$ , we need to know  $C_{gs}$  and for the devices used this led to a value  $L_g = 14.3$  nH, which is somewhat large. Therefore, we decided to use a stacked inductor because the mutual inductance of the structure will increase its overall inductance thereby allowing a smaller amount of on-chip area to be used to build it. Normally such a large inductor value would be implemented using bondwire.

Computation of the output inductor would require the knowledge of the total capacitive loading. For our analysis, we have assumed that this capacitance due to the mixer (the load as seen by the LNA) is 1 pF which will resonate with the inductor  $L_l$  at 1.9 GHz. The  $L_l$  value is then 4.7 nH. This value can be changed appropriately for a different capacitive load.

Completing the design requires specification of the DC blocking capacitor, which we selected as 10 pF. The cascoding transistor is chosen here to have the same width as the main device. This choice is somewhat arbitrary and thus not necessarily ideal. Two considerations have constrained the size of the cascoding transistor. The gate-drain capacitance can reduce the impedance looking into the gate and the drain of  $M_1$  considerably, degrading both the noise performance and input match. To suppress these consequences of the Miller effect, we would normally desire a relatively large cascoding device in order to reduce the gain of the common-source transistor. However, the parasitic source capacitance associated with a large device effectively increases the amplification of the cascoding device's own internal noise at high frequencies. As we have merged the source region of the cascoding transistor with the drain region of the common-source device (by making these two devices the same size), we have in effect reduced many of these problems.

The entire circuit schematic used is shown in figure 3. Differential configuration was used as the single ended ar-

chitecture is sensitive to the parasitic ground inductance. As seen from the figure, the ground return of the signal source is supposed to be at the same potential as the bottom of the source degenerating inductor. However, there is inevitably a difference in these potentials because there is always some nonzero impedance between these points. Since  $1.6 \text{ nH}$  for  $L_s$  is not a large inductance, small amounts of additional parasitic reactance between the grounds can have a large effect on amplifier performance. In the differential configuration, the incremental ground at the symmetrical point is exploited (i.e. the point at where the source degenerating inductances return to a virtual ground). Any parasitic resistance in series with the inductance is irrelevant. The real part of the input impedance is controlled only by  $L_s$  and is unaffected by parasitics in the ground return path. Another important attribute to the differential connection is its ability to reject common-mode disturbances. To maximize common-mode rejection at high frequencies, it is critically important for the layout to be absolutely as symmetrical as possible. Lastly, the linearity is improved in this configuration as the input voltage is divided between two devices.

### C. Note on the inductors

The inductors used in our LNA were stacked inductors. Stacked inductors have a number of advantages over basic planar inductors. They offer the possibility of

1. higher Q value
2. less on-chip area used to build them
3. higher self-resonance frequency.

The stacked inductors used in our LNA design were built in the metal 4 and metal 5 layers. These layers had the lowest parasitic elements associated with them due to their larger distance from the substrate (reduced capacitance) and larger metal linewidths (lower series resistance). The main goal to consider when modelling the inductors was to lower the parasitic elements, particularly the series resistance as this would lower the overall noise figure of the LNA. Another concern in building the inductors was the die area used. The stacked inductor's inductance is increased by approximately  $n^2$ , with  $n$  being the number of levels used in the stacked structure (i.e.  $n = 2$  for stack using metal levels 4 and 5). The inductor  $L_g$  is typically implemented using the chip bond wires. However for simulation purposes, we assumed it would be implemented as an on-chip inductor and modeled it using *ASITIC*.  $L_g$  is usually implemented by the bond wires because its large inductance value means it would require a large on-chip area to implement. The other inductors,  $L_s$  and  $L_l$ , were also modelled as on-chip inductors, which they usually are. A  $\pi$ -model was used as the equivalent circuit element to model the inductors in Spectre (see figure 5). The physical layout of the stacked inductors can be seen in figure 6.

## III. PERFORMANCE

We now present the results of the simulation of the circuit and compare the performance to the given specifications. Firstly a remark should be made on the fact that

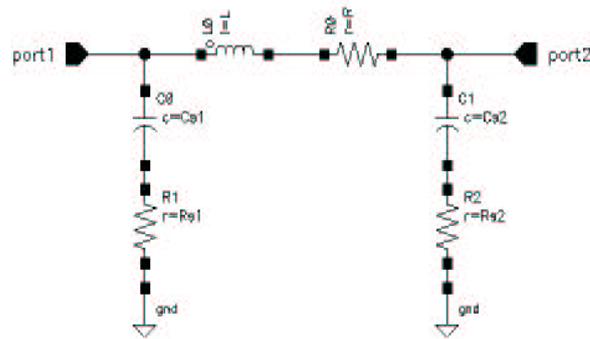


Fig. 5. Equivalent pi-model used for inductors in LNA simulator.



Fig. 6. Physical layout of stacked inductor structure.

performance of the isolated LNA is difficult to characterize, and should be optimized depending on the load presented by the following mixer. In these simulations, two types of loads were used: a purely capacitive load of  $1 \text{ pF}$ , to be tuned out with the help of the output inductor, and a more complex load composed of the capacitor of  $1 \text{ pF}$  in parallel with an resistor of  $500 \Omega$ , as the mixer also presents a resistance to the LNA. This value was chosen a posteriori to decrease the gain of the LNA and meet the specification for distortion.

### A. Input Matching

The first constraint on the LNA was to assure that the input impedance matches the source impedance, i.e. the LNA presents a purely resistive load of  $50 \Omega$  to the antenna, in order to maximize the power transfer. In order to verify this, we simply compare the phase and amplitude of the voltages at the source and at the input of the LNA, as shown on figure 7.

The simulation plots for the amplitude and phase of these signals are shown in figure 8. We can see that the

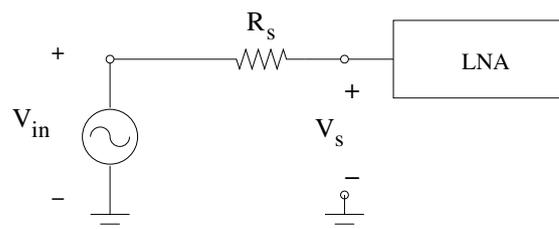


Fig. 7. Set-up for the verification of the input matching.

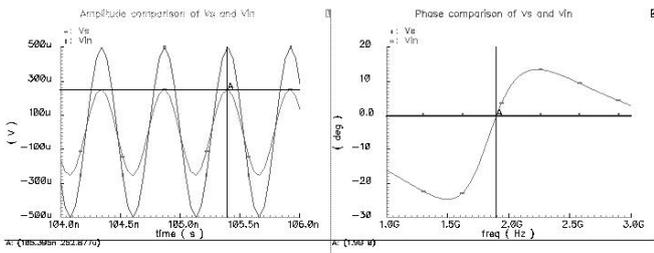


Fig. 8. Amplitude and phase of the voltage of the source and in front of the LNA.

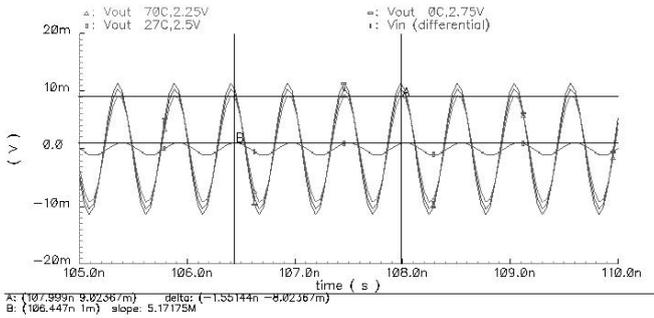


Fig. 9. Transient response of the LNA, for different supply voltage and temperature conditions. Purely capacitive load  $C = 1pF$ .

impedance looking from the input of the LNA is perfectly real (phase  $0^\circ$  at  $1.9 GHz$ ) and the amplitude of the source  $V_{in}$  is divided by 2 at the input of the LNA as expected. When the supply voltage varies by 10% there is no visible modification of the amplitude matching, while there is a maximum phase shift of  $2.5^\circ$  at  $70^\circ C$  and  $2.25V$ .

**B. Gain**

The gain of the LNA is measured in ac and transient analysis, at nominal and over supply variations between  $2.25V$  and  $2.75V$  and temperature variations between  $0$  and  $70^\circ C$  (note that the gain is measured with respect to  $V_{in}$  of the source). The worst case is given for a voltage supply of  $2.25V$  and a temperature of  $70^\circ C$ , where the gain is  $19.7dB$ . At a temperature of  $27^\circ C$  and supply voltage of  $2.5V$ , the gain is  $20.6dB$ . Therefore the specification of  $15dB$  is met even in the worst case. Note, however that this result depends on the output load. With a smaller capacitive load, we were able to increase the gain substantially (with one appropriate value of the output inductance). If we add a resistor at the output, the gain drops. We will discuss this in more detail when we talk about the distortion.

**C. Noise figure**

The noise figure was also simulated for the supply and temperature variations. The simulation used a purely capacitive load of  $1pF$  again. The noise figure was found out to be  $2.37dB$  in the worst case ( $2.25V, 70^\circ C$ ), but only  $2dB$  at nominal  $T = 27^\circ C, V_{dd} = 2.5V$ . Figure 10 shows the results of the noise simulation with Spectre.

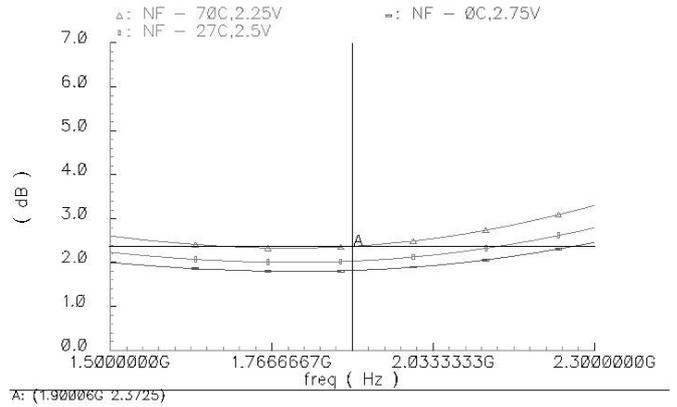


Fig. 10. Noise figure of the LNA, for different supply voltage and temperature conditions. Purely capacitive load  $C = 1pF$ .

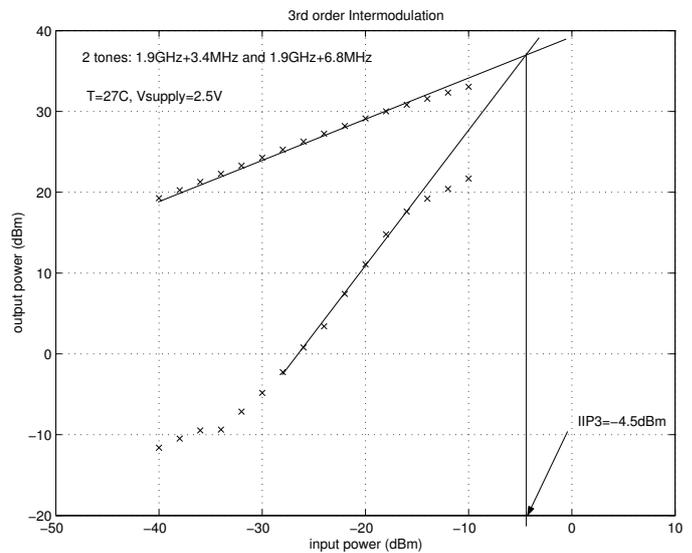


Fig. 11. Input referred IP3 of the LNA. The simulation was done using two tones separated by  $3.4MHz$ . The output load is a capacitor  $C = 1pF$  in parallel with a resistor  $R = 500 \Omega$ .

**D. Distortion**

Before we examine the distortion, let us rediscuss the problem of the load. To compute the distortion, we added a resistive load of  $500\Omega$  which reduced the gain. We chose this resistance so that the gain in the worst case ( $2.25V, 70^\circ C$ ) still meets the specification (we have a gain of  $15.7dB$  in this case). This resistor could potentially degrade the noise performance, but as it is not a part of the LNA, we have not considered it to contribute to the noise. However, we used it to evaluate the distortion of the LNA because this block works in practice with the mixer as a load. The curves for the input referred third order intermodulation intercept point are given on figure 11. There is a slight decrease in the IIP3 with variations in the supply voltage and temperature, but this is not significant, and the intercept point remains well below  $-10dBm$ .

TABLE II  
PERFORMANCE OF THE LOW NOISE AMPLIFIER.

Load		$T = 27^{\circ}C, V_{dd} = 2.5V$	$T = 70^{\circ}C, V_{dd} = 2.25V$	$T = 0^{\circ}C, V_{dd} = 2.75V$
$1pF$	Gain	$20.6dB$	$19.7dB$	$21.3dB$
	Noise Figure	$2dB$	$2.37dB$	$1.8dB$
$1pF,$ $500\Omega$	Gain	$16.6dB$	$15.7dB$	$17.2dB$
	IIP3/-1dB	$-4.5dBm / -11.5dBm$	$-4dBm / -11dBm$	$-7dBm / -12dBm$
Power Consumption	$23mW$ at $27^{\circ}C, 2.5V$ ; $25mW$ at $70^{\circ}C, 2.5V$ (PTAT current)			
Die Area	$0.23mm^2$ (the gate inductor is $400\mu m \times 400\mu m$ )			

### E. Summary

Table II summarizes the major characteristics of the circuit. Note that the power consumption is only  $23 mW$  at nominal. This is to ensure that we match the specification of a power consumption under  $25 mW$ , even at  $70^{\circ}C$ . However, we do not match this specification if the power supply becomes  $2.75V$ .

## IV. CONCLUSION

We have designed a low noise amplifier for a DECT receiver in a  $0.25\mu m$  CMOS process. We met all the specifications given to us except the power consumption for a +10% variation in the supply voltage. The noise performance was well satisfied using the MOS models provided to us. However, improved noise models which include the induced gate noise would be useful to best characterise the circuit, as this component of noise could dominate the output noise of real amplifiers.

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