Design and Implementation of a Baseband WCDMA Dual-Antenna Mobile Terminal

Jean-François Frigon, Ahmed M. Eltawil, Eugene Grayver, Alireza Tarighat, and Hanli Zou

Contact information of corresponding author:
Jean-François Frigon
Department of Electrical Engineering
Ecole Polytechnique de Montréal
C.P. 6079 succ. Centre-ville
Montréal, Québec
H3C 3A7
Canada
j-f.frigon@polymtl.ca
Tel: 514-340-4711 x3642
Fax: 514-340-5892

ABSTRACT
The design and implementation of a baseband WCDMA dual-antenna mobile terminal system on a chip (SoC) is presented in this paper. Spatial diversity processing mitigates wireless channel impairments and is a key enabling technology for WCDMA to support high quality of service at high data rates and capacity. The SoC integrates the baseband transceiver, coding and decoding functions, micro-controllers to implement the radio access protocols, and external interfaces to communicate with the application layer. The receiver design, which takes advantage of diversity benefits in several blocks, is described in detail. The SoC was fabricated in a 0.18μm, 1.8V CMOS technology and requires a total area of 72mm² consuming 532mW at the maximum data rates. The ASIC was used in lab testing where a gain of up to 9dB was observed for the dual antenna receiver, which demonstrates the tremendous improvement provided by spatial diversity. The results presented in this paper provide a base architecture and a performance benchmark for commercial implementations of WCDMA mobile terminals.

Keywords: Wideband CDMA; System on a Chip; Diversity; Baseband Modem; Smart Antenna Processing.
Footnotes

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Affiliation of authors:

J. F. Frigon is with the Electrical Engineering Department, École Polytechnique de Montréal, Montréal, Québec, H3C 3A7, Canada (e-mail: j-f.frigon@polymtl.ca).

A. M. Eltawil is with the Electrical Engineering and Computer Science Department, University of California, Irvine, CA 92697, USA (e-mail: aeltawil@uci.edu).

E. Grayver is with the Aerospace Corporation, El Segundo, CA 90245, USA (e-mail: eugene.grayver@aero.org).

A. Tarighat was with the Electrical Engineering Department, University of California, Los Angeles, CA 90095, USA (e-mail: tarighat@ee.ucla.edu). He is now with Wilinx, Los Angeles, CA 90025, USA.

H. Zou is with Broadcom Corporation, Irvine, CA 92612, USA (e-mail: hzou@broadcom.com).

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Jean-François Frigon, Ahmed M. Eltawil, Eugene Grayver, Alireza Tarighat, and Hanli Zou, Member, IEEE

Abstract—The design and implementation of a baseband WCDMA dual-antenna mobile terminal system on a chip (SoC) is presented in this paper. Spatial diversity processing mitigates wireless channel impairments and is a key enabling technology for WCDMA to support high quality of service at high data rates and capacity. The SoC integrates the baseband transceiver, coding and decoding functions, micro-controllers to implement the radio access protocols, and external interfaces to communicate with the application layer. The receiver design, which takes advantage of diversity benefits in several blocks, is described in detail. The SoC was fabricated in a 0.18μm, 1.8V CMOS technology and requires a total area of 72mm² consuming 532mW at the maximum data rates. The ASIC was used in lab testing where a gain of up to 9dB was observed for the dual antenna receiver, which demonstrates the tremendous improvement provided by spatial diversity. The results presented in this paper provide a base architecture and a performance benchmark for commercial implementations of WCDMA mobile terminals.

Index Terms— Wideband CDMA; System on a Chip; Diversity; Baseband Modem; Smart Antenna Processing.

I. INTRODUCTION

THIRD generation (3G) cellular networks [1] offer voice and data based services to wireless mobile users in large areas. Data rates and Quality-of-Service (QoS) expected by users will be comparable to those offered by conventional wired networks. However, wireless channel impairments such as fading and multipath propagation make it difficult to meet the user expectations in the entire service area. Furthermore, these wireless systems have to meet a tight power budget, maximize the number of users, and provide small and low cost handsets, which present additional design challenges. Spatial diversity is an effective tool to solve the problem of providing the desired QoS with a small cost and complexity overhead for the mobile terminal [2]. Recent advances in RF circuit techniques and integration [3] have made implementation of a smart antenna mobile receiver feasible. This paper presents the system and VLSI design of a Wideband Code Division Multiple Access (WCDMA) dual antenna mobile terminal, and its implementation on a system on a chip (SoC).

In the early development stages of wireless receivers, the design focus is on specific blocks, such as the RAKE receiver [4][5], which leads to a complete transceiver design [6]-[8]. However, these are far away from a final implementation for a mobile terminal and lack support for several functionalities, such as the physical layer management logic, coding and decoding functions, radio link control (RLC) layer, medium access control (MAC) layer, radio resource control (RRC) protocol, and external interfaces. Furthermore, several are implemented using a mixture of FPGA, DSP and micro-controllers [9][10]; which is not optimal for a low power, small area, and low cost implementation required for handsets. An alternative approach to the application specific integrated circuit (ASIC) is to use a software defined radio (SDR) flexible architecture [11]. However, the SDR architecture can not meet the stringent requirements of mass market handsets.

We have developed an ASIC which implements a single mode WCDMA dual-antenna baseband modem. The SoC provides the physical layer, coding layer, RLC, MAC, RRC, and other functionalities related to the radio aspects of a user equipment (UE) [12]. Several interfaces are also integrated to communicate with the application layer. A dual antenna diversity receiver provides several theoretical benefits, as described in Section II. The baseband transceiver design and architecture, which takes advantage of diversity in several receiver blocks to improve the system performance, is described in Section III. The baseband transceiver was integrated, as discussed in Section IV, with customized coding blocks, micro-controllers for control and monitoring of the transceiver and higher layers functionalities, and external interfaces. The system was fabricated in a 0.18μm, 1.8V CMOS technology and tested in the lab using a channel emulator. ASIC statistics and test results for dual-antenna reception are given in Section V. Implementation tradeoff of a dual-antenna architecture are also highlighted in Section V.

Similar systems implementing a baseband WCDMA mobile terminal have only been reported by the industry (e.g., MSM6280 by Qualcomm [13], BCM2152 by Broadcom [14], MWC300-30 by Freescale Semiconductor [15], OMAPV2230 by Texas Instruments [16], and SoftFone-W by Analog Devices [17]). All of these systems integrate on a single chip: a specific hardware accelerator for the WCDMA baseband transceiver (some chips are also multimode and include GSM, GPRS EDGE, HSDPA and GPS accelerators), one or two micro-controllers (the ARM9 and ARM11 micro-controllers are mostly used), multimedia accelerators and various external interfaces. Several chips also integrate an intermediate frequency interface, the analog data converters, and one or more DSP’s for modem and/or multimedia functions. Only the Qualcomm chip is offering a two antenna receive diversity architecture. However, it is important to note that since these chips are commercial, little information is available apart from top-level block diagrams and marketing brochures. This paper aims at filling this information void. The transceiver and SoC

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design presented in this paper offer a base architecture for future commercial implementation of WCDMA UE ASICs and the test results can be used as a benchmark for available and future implementations.

II. DIVERSITY

The WCDMA link quality from the base station to a mobile user can be greatly improved by using appropriate diversity techniques. In typical indoor and urban outdoor environments, the signal strength displays large fluctuations over short distances on the order of a few wavelengths. In such an environment, two antennas separated by at least half a wavelength (6.9 cm to 7.8 cm for WCDMA downlink frequency bands) receive uncorrelated signals [2]. If the antenna spacing is not practical, polarization diversity can also be used to implement a two branches diversity receiver. Algorithms using diversity techniques exploit the random nature of the propagated signal and the independence between the received signals to improve both the average power of the effective waveform as well as reduce its variance.

For a fixed number of users, using diversity techniques results in lower transmit power at the base station. For example, assume that we want to serve 99% of the users trying to access the network in a Rayleigh fading environment. Fig. 1 shows the required transmit power from the base station for this scenario if all users have either one or two antennas. It can be seen that, for a fixed capacity, the base station needs to transmit approximately 7 dB less power in the case where 2 antennas receivers are used. Equivalently, for a constant transmit power, the capacity increases by a factor of 5.

The impact of diversity on the performance of a WCDMA cellular system is further illustrated in Fig. 2 which shows the number of 12.2 Kbps voice terminals that can be supported by the system as a function of the number of 144 Kbps data users for the WCDMA standard channel case 1 [12]. In these theoretical simulations, all the data users were assumed to use either a single or a dual antenna receiver and all the voice terminals were using a single antenna receiver. We can observe the significant improvement in capacity provided by using a diversity enabled data receiver. For example, if we have 5 data terminals with single antenna receiver, only a single voice user can be supported by the system, while if the data terminals are using dual antenna receivers the network can still support 12 voice users.

III. TRANSCEIVER DESCRIPTION

A. Receiver Overview

Fig. 3 depicts the top-level block diagram of the diversity enabled WCDMA modem. The receiver processes the incoming analog signals from the two antennas to compute the soft decision allowing the decoding of the bits transmitted from the base station with the lowest probability of error. Dual antenna processing is inherent in most algorithms to improve their performance and enhance immunity to signal fading. All dedicated signal processing functions are configured and monitored by a global controller.

The received RF signal from each antenna is first down-converted to baseband, scaled using a variable gain amplifier (VGA) to appropriately load the analog to digital converter (ADC) and sampled at 4 times the chip rate with a precision of 6 bits. Note that the RF and analog sections are not treated in this paper and are not included in the baseband SoC described in this work. The digital processing begins with the 29 taps matched square-root raised cosine filters (SRRCF’s) that were implemented using canonic signed digit (CSD) format numeric representation to conserve power [18]. Following the independent filtering of both received digital signals, the frequency tracking unit output signal is used to derotate the signals in order to remove the frequency offset between the received signal and the local reference. The data streams are then linearly interpolated by a factor of 2 and compensated for the sampling frequency error. It is critical to mitigate the effects of sampling frequency error as early as possible in the datapath since it can represent a multipath position drift of up to 0.384 chips per frame, or 3.072 samples per frame, for a 10 ppm error. This can cause major problems for the operation of the cell acquisition algorithm and the multipath searcher. Note that the carrier frequency and sampling frequency control

![Fig. 1. Required node-B Tx power as a function of the number of users.](image1)

![Fig. 2. Number of voice users as a function of the number of data users.](image2)
loops are entirely digital to decrease the component cost and improve the system performance (lower loop delay, greater controllability and precision improvement). The drawback of a digital loop is the reduction in dynamic range. However, the digital loops were designed to handle an offset of up to 15 ppm, which is sufficient for commercial use.

The 8 times over-sampled signal at the interpolator output, after acquisition of the first base station, is compensated for the carrier and sampling frequency errors. The synchronized signal is then presented, for chip level processing, to the cell acquisition processor, multipath searcher and correlation engine. The cell acquisition processor and multipath searcher are discussed in sections C and D, respectively. The correlation engine is a programmable bank of correlators and is described in Section E. Once a symbol is descrambled and despread in the correlation engine, its value and the appropriate tagging information (identifying which multipath it belongs to, symbol number, etc.) is transferred to the RAKE and antenna combiner unit described in Section E. This unit computes the soft decision of the transmitted bits that are used for symbol level processing and decoding. The combiner unit is also responsible for computing the channel estimate used for various measurements and provides feedback to the frequency tracking loop and the individual multipath timing tracking loops. The RAKE receiver hardware configuration is designed to be scalable in resources. As processing requirements are increased (e.g. more multipath within an environment), more correlation engines can be activated. The particular implementation described in this paper provides a total of four correlation engines with 25 correlation resources each.

The operation of the receiver can be briefly described as follows. Once initial synchronization with a base station to within one chip period is achieved, fine frequency and timing tracking loops are initiated to lock onto the detected multipath. The multipath searcher is then configured to scan for new multipaths and updates the controller. RAKE fingers are assigned to the appropriate detected multipaths for each antenna by the controller and the combiner unit is configured to process the correlator outputs. The cell acquisition processor and multipath searcher are then configured to search and monitor new base stations and multipaths.

B. Control Loops

1) Automatic Gain Control (AGC)

The purpose of the AGC algorithm is to assure a proper loading of the ADC’s. This is accomplished by monitoring the two digital data streams after the ADC and controlling the VGA in each analog receive chain. It is reasonable to assume that for multiple antenna communication systems the noise and interference power at each receive antenna is approximately the same. The same gain is thus applied to each receive chain in order to obtain a similar noise power level at both ADC’s. This is done to simplify the design of the combiner algorithm (see Section E). Let \( x_{k,n} \) be the digital complex sample output at instant \( k \) for the ADC’s (I and Q) associated with antenna \( n \). To avoid signal saturation on any of the two receive path, the AGC algorithm is using the following metric

\[
y = \max \{ P_1, P_2 \} \text{ where } P_n = |\text{Re}(x_{k,n})|^2 + |\text{Im}(x_{k,n})|^2,
\]

which is compared to a threshold, low-pass filtered and used to control the analog VGA stages in both receive chains. Note
that since the goal is to obtain an equal overall gain in both analog chains, the VGA control signals must be corrected by the appropriate calibration factor for each receive chain.

2) Frequency Tracking Unit

The local reference signal used to down-convert the RF signal received from each antenna to baseband is derived from a common crystal. The carrier frequency offsets for both complex baseband signals are thus the same. The filtered signals are derotated by multiplying with the direct digital frequency synthesizer (DDFS) complex output signal from the frequency tracking unit. The goal of the frequency recovery loop is to remove the carrier frequency offset while the phase error is compensated in the combiner since it is multipath and antenna dependent, unlike the frequency offset. Diversity is incorporated in the frequency recovery loop by using the strongest multipath from each receive antenna to compute the frequency error. The phase difference between successive pilot symbols is employed to detect, for each antenna, the rotation direction due to the frequency offset. Equal gain combining is used to combine the rotation direction from each antenna and a hard decision is made. Denote the pilot symbol $i$ for antenna $n$ by $p_{i,n}$. The dual antenna receiver frequency loop discriminator is then given by:

$$f_{d,n} = \text{sign}(\text{Im}ag(p_{i,n}p_{i,n}^*) + \text{Im}ag(p_{i,n+1}p_{i,n+1}^*)).$$

$f_{d,n}$ is low-pass filtered and used as the input to the DDFS.

3) Timing Tracking

Similarly to the RF mixers, the sampling clock of the ADC digitizing both received analog signals is derived from a common crystal. The sampling frequency offset experienced by both antennas is the same and is directly related to the carrier frequency offset. The controller uses the frequency offset information available from the frequency tracking loop to control the sampling frequency compensation circuit in the interpolator which uses sample swallowing or repetition to remove the sampling frequency offset error. On the other hand, the sampling phase offset (i.e., optimal down-sampling time) is different for each multipath. Also, it can not be assumed that a multipath has the same sampling phase offset on each antenna. Independent conventional early-late tracking loops are therefore used for each multipath and antenna to track the optimal down-sampling time. The early-late signal is then integrated and applied to a Schmitt quantizer to determine which sample out of the 8 input samples per chip will be used for correlation. The Schmitt quantizer was found to be necessary to minimize toggling between adjacent samples due to noise and improves the system performance by up to 5 dB.

C. Cell Acquisition

Cell search is required for initial synchronization with the WCDMA network and to search for candidate cells to perform handoffs. In the first case, referred to as initial cell search, the mobile is “free-running” and needs to find an initial cell without a priori information and to synchronize its carrier and sampling frequency with the base station. In the latter case, a priori information is available at the mobile (e.g., scrambling code and timing offset of neighbour cells) and the tracking loops are synchronized with the network. The mobile needs to detect the presence of these cells and find their exact timing offset through the target cell search. Cell search in WCDMA is performed using a three stage pipelined approach, successively identifying slot boundary, frame boundary, and the code group [19][20]. The cell acquisition processing blocks use as their input the interpolator output down-sampled by a factor of 8 to the chip rate.

1) Primary Synchronization

The goal of the primary synchronization stage is to detect slot boundaries. This is achieved by detecting the 256 chips primary synchronization channel (P-SCH) sequence transmitted at the beginning of every downlink slot. This sequence is common to all basestations. Due to the low operating Signal to Noise Ratio (SNR), the matched filter output has to be averaged over several slots to get a reliable result. Furthermore, during the initial cell search, the frequency offset at the receiver can be relatively large, resulting in a significant loss if the correlation is performed coherently. To compensate for the frequency offset and achieve robustness, non-coherent combining of 4 successive shorter correlations of length 64 chips is performed. Since no reference signal is available during primary synchronization, non-coherent combining of the output of the P-SCH matched filter for both antenna is also performed. During a target cell search, the frequency offset is known; therefore the 256 chips P-SCH correlation does not suffer from any coherence loss. However, non-coherent combining of the two antenna outputs is still required. The output of the P-SCH matched filter is stored for the 2560 possible slot offsets and accumulated over the 15 slots in a frame. The offset with the maximum averaged value is declared as the slot boundary candidate for the second synchronization stage.

A characteristic of the 256 chips that form the P-SCH channel is that they are the Kronecker product of two codes of length 16 (denoted by PN1 and PN2) [12]. This observation leads to the hardware architecture shown in Fig. 4 where a 16-tap filter is matched to code PN1 while a memory block of size 256 is used to perform the filtering against the code PN2. In this approach, only a 16-tap shift register is used, therefore reducing the power consumed for clocking the flip flop registers and the area used for implementing it. Furthermore, for every output of the first stage matched filter, only 16 memory locations (partial correlation results) have to be updated, making it feasible to use a single memory block (to save area) and a clock rate of 16 times the chip rate (~64MHz) to update the memory locations properly. This structure leads to a 60% reduction in power consumption compared to a

![Fig. 4. P-SCH matched filter hardware architecture.](image)
direct 256 tap matched filter where each flip-flop is clocked. This is an important consideration since the unit is running at the sampling frequency of the ADC which typically runs at 4 times the chip rate. To further reduce power a differential matched filter was used in which the codes could have tertiary values of [-1,0,1] which allows correlation to be performed with half the number of multiply-add operations [20].

2) Secondary Synchronization

The secondary synchronization channel (S-SCH) consists of a sequence of 15 symbols of length 256 chips transmitted at the beginning of every slot and is repeatedly transmitted every frame. The symbols can take one of 16 values. The 15 symbols in a frame form a codeword taken from a codebook of 64 16-ary codewords. These 64 codewords correspond to the 64 code groups used in the wideband CDMA system and are chosen such that they have distinct phase shifts. Therefore, the correct frame boundary and code group can be detected by finding the transmitted codeword and its phase. The P-SCH is transmitted in parallel to the S-SCH and can be used as a known reference signal to decode the code transmitted on the S-SCH. The down-sampled sequence is therefore correlated against the primary and secondary sequence. Unlike the case for primary synchronization, maximum ratio combining (MRC), with the P-SCH as a reference, of the shorter correlations of length 64 chips for both antennas can be used to compute the likelihood metrics for each receive symbols. For target cell search, MRC of the 256 chips correlation for both antennas is used. Additional details for the secondary synchronization stage are available in [20].

3) Code Searcher

At the end of each frame, the code group and frame boundary searcher indicates the most likely code group and frame offset, as well as the timing offset of the slot boundary. The code searcher then uses the Common Pilot Channel (CPICH) to identify the cell-specific scrambling code. For the 150 blocks of 256 chips in the frame the down-sampled received signals from both antennas are correlated for 256 chips against the 8 Gold codes in the indicated code group. No convenient reference signal is available during the initial and target cell search. For initial cell search the code hypothesis testing metric is thus produced by non-coherently combining four 64 chips correlation values for each antenna.

For each symbol, the scrambling code associated with the largest decision statistic is chosen and receives one vote. The most likely transmitted scrambling is selected at the end of the frame by a majority vote over the 150 decisions. However, the detected scrambling code and frame timing is accepted only if the number of votes associated with the chosen scrambling code exceeds a threshold $T$ chosen to minimize the probability of false alarm. Otherwise, the candidate is rejected and the cell search continues. For target cell search, the carrier frequency offset is known and corrected by the frequency tracking loop. The correlation for each antenna can therefore be computed coherently over 256 chips and the outputs for each antenna are combined non-coherently.

4) Performance

Fig. 5 shows the simulated diversity impact on the average time to complete the cell search. In this simulation, the value for the ratio between the power allocated to the CPICH and the total transmit power is set to -10 dB and the value for the ratio between the power allocated to the SCH and the total transmit power is set to -12 dB. The power allocated to the SCH is equally divided between the P-SCH and the S-SCH. The performance was evaluated for a flat fading channel as a function of the geometry factor $G$ defined as the ratio between the total received power from the desired base station and the channel interference (i.e., additive white Gaussian noise and inter-cell interference). For example, if $G$ is -1.5 dB, a single antenna receiver will be able to find an appropriate cell after 10 frames (100 msec) whereas for a dual antenna receiver the same waiting time would require only -3.5 dB for $G$. Diversity thus provides a 2 dB improvement for synchronization.

D. Multipath Searcher

The WCDMA receiver employs a RAKE architecture to demodulate the received signal where a separate correlator receiver is assigned to each detected multipath (see Section E). Using additional correct multipaths provides more signal energy to the RAKE receiver while combining invalid multipaths increases the noise level. The multipath searcher unit performs a critical task by continuously monitoring the time varying channel and determining the current multipath profile. We provide a brief description of this unit in this paper and further details on its design and implementation are available in [21].

The multipath searcher algorithm consists of three pipeline stages as depicted in Fig. 6. The input for each stage consists of the oversampled output of the interpolator and is processed within one frame. Outputs are available for the next stage or
for controller usage at the end of a frame. The global objective of the multipath searcher is to maximize $P_d$, the probability of detecting a valid multipath, while minimizing the probability of false alarm $P_{fa}$, the probability of declaring an invalid multipath. The propagation channel from the base station to each of the two receiver antennas is affected by independent fading conditions. Therefore, each antenna is served by an independent instance of the multipath searcher.

During the initial multipath search, a range of offsets is scanned with a resolution of $1/2$ a chip to find a set of candidate multipaths. The correlation output energy for each offset is compared with two adaptive thresholds. In low SNR or fast fading channels, the statistic available in the initial search stage is only reliable for strong multipaths (CPICH $E_b/N_0$ > -15 dB) when the threshold is set for an acceptable $P_{fa}$. Having a provision for detecting strong multipaths during the initial stage is invaluable since these multipaths will be available for addition to the RAKE receiver within one frame of their appearance and can be used to mitigate the adverse effects of birth and death channel conditions. On the other hand, there exists no threshold that guarantees acceptable $P_d$ and $P_{fa}$ for weaker multipaths. A dual dwell search approach is thus used, where the correlator output energy is compared to a lower threshold to determine a set of candidates which will be further analyzed in the verification stage. Finally, the initial search stage provides an estimate of the background noise power to the controller to implement the decision stage of the multipath searcher and the RAKE finger management algorithm.

For each multipath candidate provided by the initial searcher stage, the multipath searcher verification stage computes an accurate power estimate. The power estimate is obtained by averaging the correlation output energy computed in 10 uniformly distributed periods. After the verification stage, the power estimate of each candidate is compared to a threshold providing a relatively high $P_d$ for average power multipaths (CPICH $E_b/N_0$ > -20 dB). These multipaths can thus be detected within two frames of the multipath searcher start. However, weaker multipaths with a CPICH $E_b/N_0$ in the range of -25 dB to -20 dB still can not be reliably detected after the multipath searcher verification stage due to low signal to noise ratio and strong cross correlation peaks.

At the end of each frame, the initial and verification stages report the offset and accurate power estimate for each candidate offset to the multipath searcher controller algorithm. These candidates are then monitored in the decision stage implemented in the controller over 3 frames so that the complete multipath profile (multipaths with CPICH $E_b/N_0$ > -25 dB) can be identified with low $P_{fa}$ and high $P_d$. The final decision on the presence of a multipath at a specific offset is made in the detection stage based on the average power and the reporting frequency for the candidates. The high detection probability of the complete algorithm is at a cost of 5 frames delay in the detection process which would have been unacceptable in fast fading and birth and death channels. The provision for reporting strong and average multipaths directly in the earlier stages is thus essential for these conditions.

E. **RAKE Receiver and Combiner**

The dual antenna WCDMA receiver combines time processing of multipaths with spatial processing of the signal received on both antennas to improve the system performance. However, the architecture design of the space-time system should be selected to fully exploit the space and time diversity. Three types of architecture can be used to combine space and time processing: (1) Antenna combining followed by time processing; (2) Time processing for each antenna signal followed by antenna combining; and (3) Joint antenna and time processing. The first architecture is not suitable for channel with large rms delay, as expected in WCDMA. The second architecture performs better in outdoor channels since it has access to the complete diversity information in the time and space domains. On the other hand, the joint space-time processing architecture simultaneously removes the inter-symbol interference and combines the signals received on the multiple receive antennas and multipaths through an MMSE combiner, for example. This architecture is slightly more complex than the second one due to more computationally intensive weight calculation but does not require more correlators and has a similar combiner structure. However, its performance is better than the 2nd architecture in the presence of colored interference. The WCDMA receiver described in this paper implements the joint space-time processing architecture. A RAKE correlator is assigned to the detected multipath on each antenna. All correlator outputs are then combined together in a single space-time combiner. The weights used in the combiner can be computed using either an MRC or MMSE algorithm.

The oversampled signals at the output of the interpolator for each antenna which have been corrected for carrier and sampling frequency offsets are distributed to the correlation engines. The correlation engine is a programmable bank of correlators where each correlator can be configured as a regular data correlator, a timing tracking correlator, or a pilot correlator. Each correlator can be independently configured to the desired type, code offset and receive antenna. Each
configuration triggers a different data flow within the correlation engine and in the interaction of the correlation engine with surrounding blocks. For optimal power management, the supervising controller has both coarse and fine control over the resources. It controls the activation sequence of the correlation engines and of the correlation resources within each block. Clock gating is used extensively to save power, any inactive resource is clock gated to minimize power consumption.

For each antenna \( i \), \( i=1,2 \), the cell searcher selects \( L_i \) multipaths and independent correlator blocks are assigned to each of these \( (L_1+L_2) \) multipaths. The multipath management algorithm allocates RAKE fingers to multipaths found by the searcher based on the power of the reported multipaths, the history of multipaths currently tracked, the availability of RAKE fingers, and the current bit error rate (BER), frame error rate (FER) and SNR.

The block diagram of a correlator block is shown in Fig. 7. The incoming signal is down-sampled to the chip rate and correlated with \( N \) orthogonal variable spreading factor (OVSF) codes to obtain the outputs for each data channel. It is also correlated with the pilot code associated with these data channels to obtain the pilot output. The oversampled signal is also used to drive the early-late timing recovery loop that controls the sampling time of the data and pilot correlators.

Fig. 8 provides a block diagram of the combiner. The pilot correlations for each multipath and antenna are used to compute the weighting coefficients for combining the data correlation outputs. For each data channel \( n \), \( k(n) \) multipaths are combined (in this context a multipath is a generic name that includes actual multipaths, multiple antennas and multiple base stations). Note that the number of combined multipaths might be adjusted on a per channel basis depending on the quality-of-service requirement and correlators available. Furthermore, the combining mode (normal, STTD or closed loop transmit diversity) can change on a per channel basis. The combiner memories are designed to accommodate multipaths within a time interval taking into account the maximum propagation delay and soft handovers. The combiner unit is also responsible for computing the channel estimate used for various measurements and providing feedback to the frequency tracking loop and the multipath timing tracking loops.

Assuming that channel \( n \) uses a spreading factor \( S \), the correlator outputs for multipath \( k \) are denoted by \( y_{n,j,k} \). \( j=0,\ldots,38400/S-1 \) and the weights available for this multipath at the instant where the correlator outputs are combined are denoted by \( w_{n,j,k} \). In normal mode of operation, the combiner soft output is then given by:

\[
\hat{d}_{n,j,k} = \sum_{t=0}^{T(n)} y_{n,j,k} w_{n,j,k}^*
\]

In this paper we will not describe the combining methods and weight computation algorithms for STTD and closed loop transmit diversity modes, due to space limitations.

Assume that the pilot correlator outputs for multipath \( k \) are denoted by \( p_{j,k} \). The weights after the \( t \)th update are denoted by \( w_{n,j,k} \). Two approaches are used to compute the combining weights: MRC and least mean square (LMS) algorithm. For MRC, multipaths are weighed proportionally to their SNR. However, the noise power levels are similar for all multipaths. We can thus directly use the channel estimates as weighting coefficients for MRC. The weights for a given multipath are updated every time a pilot correlation \( p_{j,k} \) is available for this multipath. The weight update is computed as follows:

\[
w_{n,j,k} = \beta w_{n,j,k} + (1-\beta)p_{j,k}(1-i), \quad i = \sqrt{-1}.
\]

\( \beta \) is a forgetting factor that allows the tracking of fading channels and filters the noise. Multiplication by \( (1-i) \) is required to remove the CPICH modulation to obtain the channel estimate. When LMS is employed, the weights for all multipaths are updated simultaneously every time the pilot correlations for all \( k(n) \) multipaths are available. The weight update is computed as follows:

\[
w_{n,j,k} = \beta w_{n,j,k} + \mu \text{sign}
\left( (1+i) - \sum_{t=0}^{T(n)} p_{j,k} w_{n,t,k} \right) p_{j,k}, \quad i = \sqrt{-1}.
\]

The sign function of a complex number \( c=a+jb \) is defined as \( \text{sign}(c)=\text{sign}(a)+j\text{sign}(b) \). \( \beta \) is a leakage factor and provides a better performance in fast fading channel conditions. Additional details on the combiner design and implementation can be found in [22].

Fig. 9 compares the combiner output SNR CDF for a voice user using a dual antenna receiver for MRC and LMS combiners. The simulation assumes 60 users with equally distributed power. The received Ec/No was set to 6 dB in the simulation with AWGN noise. The channel conditions were fixed and the channel profile for the 3GPP standardized channel model number 3 was used. Note that for this channel a four finger RAKE receiver is used for each received antenna. It can be easily observed from these results that for this channel, a receiver using an LMS algorithm offers an improvement of approximately 1.5 dB over a conventional MRC receiver. Furthermore, for these simulations, the inter-cell interference was modeled as white noise. However, in a real system, the inter-cell interference is colored. Under these conditions, the LMS improvement would be more significant.
**F. Transmitter**

The transmitter can either channelize encoded data bits from higher layers or generate preamble sequences for the random access procedure. The transmitter supports up to 6 parallel data channels at a spreading factor of 4, or one data channel at spreading factors of 4 to 256, in addition to the control channel. The scaling factors of the data and control channels are programmable. The complex data or preamble sequence at the 3.84 MHz chip rate is then scrambled. All scrambling sequences described in the 3GPP standard are supported.

The mobile terminal modulated carrier frequency shall be accurate to within ±0.1 PPM compared to the carrier frequency received from the base station. Furthermore, the same frequency source for both RF frequency generation and the chip clock shall be used. This is a strict requirement since most inexpensive crystal oscillators do not have very good frequency stability. Since for both the terminal and the base station the frequency sources used in the downlink and uplink are the same and the Doppler shift is the also the same, the frequency error measure in the receiver is the same as the correction required for transmission. The receiver DDFS input signal word is therefore monitored and used to configure the transmitter digital correction units. An overflowing numerically controlled oscillator (NCO) is used to generate, from the free running master clock, the synchronized chip clock controlling all transmitter units. The frequency error of the RF mixer is pre-compensated by rotating the scrambled complex sequences using a 32 points DDFS.

The signal then needs to be up-sampled by a factor of 4 and filtered using a SRRCF. This is accomplished by first up-sampling the signal by a factor of 2 and filtering using a 17-tap SRRCF followed by a 15-tap polyphase half-band filter. This implementation leads to savings of approximately 50% compared to an equivalent direct 33-tap SRRCF at 4 times the chip rate. The filtered signal is finally scaled depending on the number of data channel and clipped to reduce the peak to average power ratio. The complex signal is finally quantified to 8 bits and sent to the I and Q digital to analog converters (DAC’s) at four times the corrected chip rate.

The digital signal for the transmitter has an error vector magnitude of 4% (the 3GPP requirements is 17.5%) and the out of band emission and adjacent channel leakage power ratio are met with a minimum margin of 10 dB. When integrated with the analog and RF transmitter sections, the transmitter met all 3GPP requirements.

## IV. SYSTEM ON A CHIP IMPLEMENTATION

The dual antenna WCDMA transceiver was implemented in a SoC, which also integrates dedicated hardware blocks for coding and decoding functions, and micro-controllers to monitor and configure the modem and implement the coding and protocol layers. The SoC is described in this section, followed by an overview of the external interfaces and a description of the power management techniques.

### A. SoC Overview

Fig. 10 illustrates the overall SoC which includes the baseband modem section, the coding layer and the protocol layer of the standard. It is based on a dual embedded microcontroller architecture (ARM922T cores). The first micro-controller (PHY) performs all the physical layer control including control of the RF section and the digital modem. PHY is also responsible for performing some of the coding and decoding tasks in firmware. The second micro-controller (PRO) is responsible for protocol stack operations including communication with higher layers to establish call control as well as communication with off chip components. A dual processor architecture allows a clear separation between the physical layer code and the protocol stack code which simplifies code development and debugging leading to a robust solution. This architecture also allows the master clock frequency to be dynamically scaled depending on the computational requirements of the scenario being demodulated (e.g full rate vs. low rates) and provides an efficient global power management for the ASIC.

The combiner output symbols from the modem are 10 bits soft values. Control symbols are first extracted from the data channel and made available directly to the controller. In particular, the current transport format is determined by decoding the TFCI bits and the current SNR for the data channel is computed using the dedicated pilot bits. The SNR estimate is used to determine the scaling factor used to reduce the precision from 10 to 4 bits with optimal scaling in fading conditions for soft Viterbi and/or Turbo decoding. Symbol level processing is then performed on the 4 bits soft values.

Fig. 11.a illustrates the decoding steps as defined by the WCDMA standard. The shaded areas indicate operations that are hardware assisted by dedicated accelerator units as well as a coprocessor. The first decoding block extracts control symbols and performs data scaling and de-interleaving. Symbols are then made available to the PHY micro-controller for the following four control intensive steps up to first de-interleaving which is performed by an embedded co-processor that has access to the micro-controller internal registers. This tight coupling allows for fast execution and reduced power consumption since the controller does not have to access memory. The second decoding block then performs rate matching and Turbo or trellis decoding. Fig. 11.b illustrates
the reciprocal uplink encoding as defined by the WCDMA standard. Shaded steps indicate hardware assisted operations. The same co-processor used for downlink is reused to perform second and first interleaving as well as rate matching. Turbo encoding is performed by a dedicated hardware unit.

### B. SoC External Interfaces

The WCDMA transceiver can be used in a number of different configurations and thus requires different interfaces (e.g. CardBus, USB, OMAP serial, UART) for the relatively high data rates. The ASIC implements a general purpose data port that can be adapted for use with different standards. The data port implements a full SRAM-type interface with both master and slave modes. The PRO can master the interface to read/write data from a slave device. Alternatively, an external device can treat the transceiver as a simple memory mapped device by mastering the port and writing directly to internal memory. The memory buffer is large enough to hold 10ms worth of receive and transmit data as well as control information. A standard serial interface (SPI) is used to control the analog/RF front end, and additional GPIOs are used to control non-standard components.

The high data rates required by WCDMA combined with the complexity of the protocol layer result in memory requirements that are much higher than for previous generations of standards. The ASIC interfaces to an external FLASH and an external DRAM. The FLASH holds the software for both the protocol and physical layers. However, running the software out of the relatively slow FLASH is not feasible at high data rates. Instead, the code is copied to the much faster DRAM and run from there. At the highest data rates, the code and the data use over 4MB of memory. To save power during low data rate conditions the external SDRAM is switched off and the code can run from Flash.

### C. Power Management Techniques

One of the main goals of the design was to provide aggressive means of power control since most 3G applications are power hungry. To address these issues we utilized power control methods that can be broadly categorized into distributed and centralized methods. These techniques are in addition to the power saving modes mentioned before, namely, dual processor architecture and hardware assisted processing.

Fine grained clock gating was inserted at the synthesis level to disable the clock to each group of flip-flops with a constant output. Banks of registers that exceed four flip flops in depth have been gated. This approach minimizes both the clock load capacitance and register switching but requires a large number of clock gates. Careful analysis was performed to ensure that the total capacitance of the inserted clock gates is much less than the gated registers to reap the power savings benefit. This methodology is important since as the complexity of the design increases the number of clock gates and their drive strength increases which defeats the purpose of power savings.

Centralized schemes on the other hand are managed by the microcontroller and affect the entire SoC. These are divided into two approaches:

- **a) Centralized clock gates** for entire blocks can be gated on or off by writing an instruction from the micro-controller to a control register. This coarse clock-gating is important to complement the distributed clock gating since the clock gating elements will be clocked regardless of whether the subsequent logic is active or not. By providing a master clock gate for blocks the distributed clock gating structures within that block are not clocked.

- **b) Ability to maintain functionality over a wide range of master clock frequencies**. Rather than fix the master clock frequency at which the chip can provide functionality, it was our goal to design the chip such that there is a gradual and fine-grained reduction in computational capacity as a function of the frequency. Thus by predicting the anticipated computational load, substantial power gains can be achieved by operating the chip at a reduced frequency. The ASIC was designed to run at a nominal frequency of 100 MHz, however it maintains functionality for the range of frequencies from 64 MHz (12 RAKE fingers 384 Kbps downlink) up to 100 MHz (20 RAKE fingers, 2 Mbps downlink). An integrated PLL is used to provide the required frequency granularity.

### V. PERFORMANCE EVALUATION

The SoC was implemented in a 0.18 μm, 1.8 V CMOS technology. Table I presents the statistics of the physical chip implementation, while the die photo is presented in Fig. 12. The chip is mostly dominated by the two controllers and the memory required for frame buffering at high data rates. Table II presents a detailed breakdown of the different blocks. As indicated in the table, the dual antenna operation only affects

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the RAKE receiver section since after the combiner all contributions from both antenna are merged into symbols.

Table III isolates the statistics of the RAKE receiver itself and indicates the area breakdown of the RAKE engine major components. Although, it is difficult to isolate the exact overhead associated with dual antenna processing, it is clear that relatively to the entire SoC the overhead is acceptable. For example, assuming the worst case of complete replication of hardware for a dual antenna solution versus a single antenna solution, the overhead in power is 40 mw which is 7.3% of the total power of the SoC, while the area overhead is 4.4% of the entire SoC area. This is a pessimistic estimate since a large proportion of the logic that processes one antenna is re-used for the dual antenna case, however it is useful to achieve an upper bound on the associated overhead.

To measure the performance of the SoC under realistic wireless conditions, a test setup incorporating a WCDMA signal generator, a wireless channel emulator, a reference board including the SoC, and a PC was built. In this setup, a standard conforming WCDMA signal is generated, upconverted to RF and passed at RF to the channel emulator. The channel emulator output signal is presented at RF to a board incorporating the SoC described in this paper. The board includes RF, analog and digital sections designed with commercially available components. In particular, RFMD chip sets [23] were used for the up and down conversion chains and Maxim ADC’s and DAC were used [24]. BER and receive statistics are reported from the SoC to the PC for monitoring.

Fig. 13 illustrates the test results for single and dual antenna under flat fading conditions, at a speed of 3 Km/h, with a SNR of -9 db and a 384 Kbps DCH. The experimental results show a significant improvement of 9 dB between dual and single antenna processing that at 1% BLER. To validate the performance under multipath fading channel conditions, experimental tests were setup for selected 3GPP configurations [12] and tested at 1% BLER. Table IV summarizes the results and compares with end-to-end...
simulations results of the proposed dual antenna WCDMA mobile receiver. The test results confirm the simulation results and clearly demonstrate the performance improvement provided by using a dual antenna receiver. Depending on the scenario, the gain varies from 2.5 dB to 10 dB. For example, for the 3GPP test case 2 at 12.2 Kbps, a dual antenna receiver would allow a base station to reduce the power allocated to the dedicated data channel by 6.7 dB. The base station will thus be able to support more users. Alternatively, a dual antenna receiver could tolerate a 6.7 dB stronger interference for the same power allocation, thereby extending the coverage area.

VI. CONCLUSIONS

A complete SoC for a WCDMA dual antenna mobile terminal was introduced in this paper. The receiver was designed to take advantage of the available spatial diversity in several key blocks to improve the system performance. The main receiver algorithms and implementation architectures were described. Details of the SoC integration and design were also given. The SoC was fabricated in a 0.18 μm, 1.8 V CMOS technology. It occupies a total area of 72mm² and consumes 550mW at the maximum data rates. The ASIC was integrated in a test platform for performance validation. The UE was standard compliant and measurements confirmed the significant improvement that can be provided by a dual antenna receiver in a WCDMA environment.

REFERENCES